

<b>Form PTO-1449</b> (Rev. 8-83)		U.S. Department of Commerce Patent and Trademark Office		<b>Atty Docket 0756-2156</b>		<b>Serial No. 09/542,473</b>	
<b>INFORMATION DISCLOSURE STATEMENT</b>				<b>Applicants:</b> Takayuki IKEDA			
				<b>Filing Date:</b> April 04, 2000		<b>Group Art Unit:</b> 2826	
<b>U.S. PATENT DOCUMENTS</b>							
Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)	
AS	6,013,929	01/11/2000	Ohtani				
<b>OTHER DOCUMENTS</b> (Including Author, Title, Date, Pertinent Pages, Etc.)							
Examiner Initial							
AS	Specifications and Drawings for Application Serial No. 08/862,895, "Semiconductor Intergrated Circuit and Fabrication Method Thereof", Filing Date: May 23, 1997, Inventor: Hisashi OHTANI						
AS	Specifications and Drawings for Application Serial No. 09/468,859, "Thin Film Transistor, Method of Manufacturing the Same, and Semiconductor Device Including the Same" Filing Date: December 21, 1999, Inventor: Hisashi OHTANI						
	Specifications and Drawings for Application Serial No. 09/487,432, "Semiconductor Device and Process for Production Thereof" Filing Date: January 19, 2000, Inventors: Shunpei YAMAZAKI et al.						
	Specifications and Drawings for Application Serial No. 09/493,411, "Semiconductor Device and Method of Fabricating the Same" Filing Date: January 28, 2000, Inventors: Shunpei YAMAZAKI et al.						
Examiner <u>AS</u>				Date Considered <u>5/18/03</u>			
*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							